WHAT IS CLAIMED IS:

Sub B7

1. An contact structure between a memory cell capacitor and a transistor active area within a semiconductor substrate, said contact structure comprising:

a conductive filler interposed between said active area and said memory cell capacitor; and

a silicon nitride spacer surrounding sidewalls of said conductive filler.

2. The contact structure according to Claim 1, wherein said conductive filler comprises a transition metal.

3. The contact structure according to Claim 1, wherein the transition metal is selected from the group comprising platinum, rhodium, palladium, iridium and ruthenium.

4. The contact structure according to Claim 1, wherein said conductive filler comprises a conductive oxide.

5. The contact structure according to Claim 1, further comprising an active area cladding forming ohmic contact between said contact plug and said active area.

6. The contact structure according to Claim 5, wherein said cladding comprises a silicide layer.

7. The contact structure according to Claim 5, further comprising a conductive barrier layer formed between said cladding and said conductive filler.

8. The contact structure according to Claim 7, wherein said conductive barrier layer comprises titanium nitride.

9. The contact structure according to Claim 7, wherein said conductive barrier layer comprises tungsten nitride.

10. The contact structure according to Claim 1, further comprising a conductive diffusion barrier between said conductive filler and said silicon nitride spacer.

11. The contact structure according to Claim 10, further comprising a conductive barrier cap layer interposed between said conductive filler and said memory cell capacitor.

12. The contact structure according to Claim 1, having a width of less than or equal to about 0.40 μm.

13. The contact structure according to Claim 1, wherein said memory cell capacitor comprises a capacitor dielectric having a dielectric constant greater than about 20.

14. The contact structure according to Claim 13, wherein said capacitor dielectric comprises a complex oxide.

15. The contact structure according to Claim 14, wherein said capacitor dielectric is selected from the group consisting of tantalum oxide, barium strontium titanate, strontium titanate, barium titanate, lead zirconium titanate, and strontium bismuth tantalate.

16. An integrated circuit, comprising:

a semiconductor substrate having a transistor active area formed therein;

a transistor gate formed over the substrate;

a contact plug in electrical contact with the active area, the contact plug extending over the substrate;

an insulating spacer surrounding sidewalls of the contact plug;

an interlevel dielectric having a different composition from the insulating spacer surrounding the insulating spacer; and

a capacitor formed over and in electrical contact with the contact plug, the capacitor incorporating a material having a dielectric constant of greater than about 10.

17. The integrated circuit of Claim 16, wherein the contact plug comprises a metallic filler material.

18. The integrated circuit of Claim 17, wherein the filler material comprises a transition metal.

19. The integrated circuit of Claim 18, wherein the filler material comprises a conductive metal oxide.

20. The integrated circuit of Claim 17, wherein the contact plug further comprises a conductive barrier layer interposed between the insulating spacer and the filler material.

21. The integrated circuit of Claim 20, wherein the conductive barrier layer comprises a metal nitride.

22. The integrated circuit of Claim 20, wherein the conductive barrier layer further extends between the active area and the filler material.

23. The integrated circuit of Claim 20, wherein the contact plug further comprises a conductive barrier cap interposed between the capacitor and the filler material.

24. The integrated circuit of Claim 16, wherein said capacitor defines a container shape.

25. The integrated circuit of Claim 24, wherein said capacitor defines a crown shape.

26. The integrated circuit of Claim 24, wherein said capacitor defines a post shape.

27. The integrated circuit of Claim 16, wherein the insulating spacer comprises silicon nitride.

28. The integrated circuit of Claim 16, wherein the insulating spacer directly contacts a conductive layer of the transistor gate stack.

29. A system including an integrated circuit, the integrated circuit comprising:

a contact plug electrically connecting a lower circuit element and an upper circuit element, the contact plug having a lower surface contacting the lower circuit element, an upper surface contacting the upper circuit element, and a sidewall extending between the lower surface and the upper surface;

a non-conductive diffusion barrier surrounding the contact plug sidewall; and

an interlevel dielectric surrounding the non-conductive diffusion barrier.

30. The system of Claim 29, wherein the non-conductive diffusion barrier comprises silicon nitride.

31. The system of Claim 29, wherein the lower surface of the contact plug is defined by a silicide cladding over a transistor active area.

32. The system of Claim 29, wherein the upper surface of the contact plug is defined by a conductive barrier cap.

33. The system of Claim 29, wherein the upper circuit element comprises a capacitor incorporating a capacitor dielectric with a dielectric constant of greater than about 10.

34. The system of Claim 33, wherein the contact plug comprises a non-oxidizing conductive material.

35. The system of Claim 34, wherein the non-oxidizing conductive material comprises a conductive metal oxide.

36. The system of Claim 29, wherein the diffusion barrier directly contacts a conductive word or digit line.

37. A memory cell in an integrated circuit, comprising:

a capacitor having a top electrode, a bottom electrode, and a high dielectric constant dielectric between the top electrode and the bottom electrode;

a semiconductor substrate having an active area;

a contact plug between the bottom electrode and the active area, the contact plug comprising a non-oxidizing conductive material;

an interlevel dielectric layer surrounding the contact plug; and

a non-conductive spacer between the contact plug and the surrounding interlevel dielectric layer.

38. The memory cell according to Claim 37, wherein the non-conductive spacer comprises silicon nitride.

39. The memory cell according to Claim 37, wherein the high dielectric constant dielectric comprises BST.

40. The memory cell according to Claim 37, wherein the non-oxidizing conductive material comprises a transition metal.

41. The memory cell according to Claim 37, wherein the non-oxidizing conductive material comprises a conductive metal oxide.

42. An integrated circuit comprising:

at least two conductive lines separated by less than about 0.50 μm;

a contact passing between the two lines; and

an interlevel dielectric layer covering the lines,

at least a section of the conductive lines directly contacting the interlevel dielectric.

43. The integrated circuit of Claim 42, wherein the conductive lines comprise word or digit lines extending over a semiconductor substrate in a memory chip.

44. The integrated circuit of Claim 42, wherein the contact is electrically insulated from the two lines by a spacer surrounding the contact.

45. The integrated circuit of Claim 44, wherein the contact connects a transistor active area to a memory cell capacitor, the capacitor incorporating a complex oxide material.

46. The integrated circuit of Claim 44, wherein the spacer comprises silicon nitride.

47. A system including an integrated circuit, comprising:

a semiconductor substrate

a transistor gate electrode including at least one conductive layer, the gate electrode formed over the semiconductor substrate;

a transistor active area within the substrate and adjacent the gate electrode; and

a contact structure electrically contacting the active area, the contact structure including a conductive material surrounded by a non-conductive spacer, the spacer directly contacting the conductive layer of the gate electrode.

48. A process for forming an electrical interconnection between a capacitor and an active area in a semiconductor substrate, comprising:

providing an interlevel dielectric over said semiconductor substrate;

etching said interlevel dielectric to form a contact hole exposing the active area;

depositing a non-conductive layer into said contact hole;

conducting a spacer etch on said non-conductive layer to define a non-conductive liner and expose said active area in said contact hole;

depositing a conductive material within said non-conductive liner in said contact hole; and

forming a capacitor over said contact plug.

49. The process of Claim 48, wherein said conductive material comprises a non-oxidizing conductor.

50. The process of Claim 49, wherein said conductor is selected from the group consisting of platinum, rhodium, palladium, iridium, ruthenium, rhodium oxide, iridium oxide ruthenium dioxide, and combinations thereof.

51. The process of Claim 49, further comprising forming a silicide between said conductive material and said active area.

52. The process of Claim 51, wherein forming said silicide comprises:

depositing a titanium layer within said non-conductive liner in said contact hole;; and

reacting said titanium layer with said substrate.

53. The process of Claim 51, further comprising depositing a conductive barrier layer into the contact hole over the silicide layer.

54. The process of Claim 53, wherein said conductive barrier layer comprises a metal nitride.

55. The process of Claim 49, where etching said insulating layer comprises selectively etching the interlevel dielectric relative to a protective insulator over an adjacent transistor gate.

56. The process of Claim 49, wherein said capacitor incorporates a high dielectric constant material.

57. The process of Claim 56, wherein forming the capacitor includes annealing the high dielectric constant material in an oxidizing atmosphere.

58. A process of forming an integrated circuit, comprising:

forming at least two conductive lines separated by less than about 0.50 μm;

depositing an interlevel dielectric over the conductive lines, the interlevel dielectric directly contacting a sidewall portion of a conductive layer within the conductive lines;

etching a contact hole through the interlevel dielectric between the conductive lines to expose a circuit element;

forming a non-conductive spacer within the contact hole; and

filling the contact hole with a conductive material after forming the non-conductive spacer.

59. The process of Claim 58, wherein etching the contact hole comprises exposing the sidewall portion of a conductive layer within the conductive lines.

60. The process of Claim 59, wherein filling the contact hole comprises depositing a conductive barrier layer into the contact hole and filling the contact hole with a conductive filler material after depositing the conductive barrier layer.

61. The process of Claim 59, further comprising depositing a metal layer into the contact hole after forming the non-conductive spacer and reacting the metal layer with the circuit element.

62. A method of forming a contact in an integrated circuit, the method comprising:

etching a contact via through an interlevel dielectric;

lining the contact via with an insulating material; and

filling the contact via with a conductive material after lining the contact via.

63. The method of Claim 62, wherein filling the contact via comprises depositing a transition metal.

64. The method of Claim 62, wherein filling the contact via comprises depositing a conductive oxide.

65. The method of Claim 62, further comprising conducting a spacer etch after lining the contact via and before filling the contact via.